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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/654,875

09/05/2000

Isao Nojiri

50006-073

7618

7590

08/13/2004

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EXAMINER

PAREKH, NITIN

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 08/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/654,875	Applicant(s) NOJIRI ET AL.	
	Examiner Nitin Parekh	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 July 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 7-10 and 13-21 is/are pending in the application.
- 4a) Of the above claim(s) 7-9 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 10-16 and 19-21 is/are allowed.
- 6) ☒ Claim(s) 17 and 18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 September 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. The finality of the previous office action (see the final action, paper number 19 dated 02-25-04) has been withdrawn. A non-final office action is set forth below.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable Fukui et al. (US Pat. 6100594).

Regarding claim 17, Fukui et al. disclose a semiconductor device (Fig. 4-9B) comprising:

- a circuit board (Col. 6, line 31; see 5 in Fig. 4)
- a first semiconductor chip (1 in Fig. 7b/7a-8b) positioned on the circuit board
- a second semiconductor chip (1 in Fig. 7b/7a-8b) positioned on the first semiconductor chip
- the circuit board has a first pad and a second pad (see fourth and sixth pad 13 respectively from left in Fig. 7b), the second pad being spaced away from the first

pad in a direction along an outer periphery/side of the first semiconductor chip (see fourth and sixth pad 13 from the left being connected with short wires 7 to respective pads 17a on the chip 1 in Fig. 7b)

- the first semiconductor chip has a third pad, a fourth pad spaced away from the third pad (see third and fourth pad 17a respectively from left on the chip 1 in Fig. 7b) in a direction along an outer periphery/side of the second semiconductor chip, the third and fourth pads being positioned adjacent to the first and second pads, respectively
- the second semiconductor chip has a fifth pad (see third pad 17b from left on the chip 2 in Fig. 7b) positioned adjacent to the third pad but away from the fourth pad on the first semiconductor chip, and
- the first pad on the circuit board and the third pad on the first semiconductor chip and the second pad on the circuit board and the fourth pad on the first semiconductor chip are electrically connected through respective bonding wires (see 7 in Fig. 7b) and the first pad on the circuit board and the fifth pad on the second semiconductor chip being connected through two bonding wires (see 7 in Fig. 7b).

Fig. 7b; Fig. 4-8b; Col. 10, lines 30-67; Col. 6-10).

Fukui et al. further teach the first pad on the circuit board and the fifth pad on the second semiconductor chip being connected through a single bonding wire (see a long wire 7 connecting pads 13 and 17b in Fig. 7a).

Fukui et al. fail to teach the wire connecting between the third and forth pads on the first semiconductor chip.

Fukui et al. further teach another embodiment (see Fig. 9b) where a wire/trace is connected between two pads on the surface of the first semiconductor chip, the wire/trace having segments connecting the pads where the connecting segments extend in a plurality of directions including the wire/trace having an extension along and perpendicular to the outer periphery of the second semiconductor chip (see the wire/trace connecting pads 17a in Fig. 9b), such wire/trace on the circuit board being printed/patterned using a conventional metal deposition and photolithography/printing processes (Col. 7, line 30-60).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the wire connecting between the third and forth pads on the first semiconductor chip where the wire extends along the outer periphery of the second semiconductor chip as taught by the embodiment of Fig. 9b in Fukui et al. so that the bonding wire spacing can be improved and wire bonding defects can be reduced in Fukui et al's device.

4. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukui et al. (US Pat. 6100594) in view of the APA.

Regarding claim 18, Fukui et al. teach the entire structure as applied to claim 17 above, except the semiconductor device being mounted on a motherboard.

APA teaches the device having the circuit board being conventionally mounted on a motherboard (APA, specification pages 1-4).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the semiconductor device being mounted on the motherboard as taught by APA so that component density can be increased in Fukui et al's device.

Allowable Subject Matter

5. Claims 10-16 and 19-21 are allowed.

Reasons for Allowance

6. The following is an examiner's statement of reasons for allowance:

The references of record do not teach either singularly or in combination at least the limitations "the circuit board has a first pad, a second pad spaced away from the first pad in a direction along an outer periphery of the chip and a wire connecting the first pad and the second pad on the surface of the circuit board supporting the first

semiconductor chip, the wire being printed on the circuit board together with the first and second pads, and the wire extending along the outer periphery of the first semiconductor chip between the first and second pads” as recited in the independent claim 10, or “the first and second pads on the circuit board and the second pad on the circuit board and the third pad on the second semiconductor chip are electrically connected through respective bonding wires” in a device having a plurality of pads and wire bonding configuration including a first chip mounted on a circuit board and a second chip mounted on the first chip.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Art Unit: 2811

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NP

08-09-04



NITIN PAREKH

PATENT EXAMINER

TECHNOLOGY CENTER 2800